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Wayne P. Bailey
Storage Technology Corporation
One StorageTek Drive
Louisville, CO 80028-4309

EXAMINER

TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 04/09/2004

2

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/017,548

Applicant(s)

BOYER ET AL.

Examiner

Joseph D. Torres

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 December 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 December 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: '317' in Figure 3 and '514' in Figure 5. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-24 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the correction history record" in 6. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites, "the number of times errors have been found". Note: time is a relative term and it is certain that as time varies, the number of errors will change, hence without stating the relationship between time and the number, the claim is indefinite

Claim 8 recites the limitation "the correction history record" in 8. There is insufficient antecedent basis for this limitation in the claim.

Claim 14 recites, "the number of times errors have been found". Note: time is a relative term and it is certain that as time varies, the number of errors will change, hence without stating the relationship between time and the number, the claim is indefinite

Claim 15 recites the limitation "the correction history record" in 14. There is insufficient antecedent basis for this limitation in the claim.

Claim 21 recites, "the number of times errors have been found". Note: time is a relative term and it is certain that as time varies, the number of errors will change, hence without stating the relationship between time and the number, the claim is indefinite

Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. Claim 1 recites, "a limited number of the multiple tracks are decoded as erasures". See MPEP § 2172.01. The omitted elements are: the relationship between "multiple tracks", decoding and "erasures" (Note: tracks are physical structures for storing data). The Examiner assumes the following was intended: --a limited number of data along the ~~of the~~ multiple tracks are decoded as erasures--.

Claims 8 and 15 recite similar language as in claim 1, hence are rejected for the same reasons.

Claims 7, 14 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 7 recites, "the number of times errors have been found". The omitted structural cooperative relationships are: the relationship between the number of errors and time (Note: time is a relative term and it is certain that as time varies, the number of errors will change, hence without stating the relationship between time and the number, the claim is indefinite).

Claims 14 and 21 recite similar language as in claim 7, hence are rejected for the same reasons.

Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: devices necessary for a data storage device to read a data storage medium.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue; Toru et al. (US 4336612 A, hereafter referred to as Inoue).

35 U.S.C. 102(b) rejection of claim 1.

Inoue teaches a method of correcting errors in a data storage medium having a plurality of tracks (col. 8, lines 26-68 of Inoue, Note: the PCM multi-track digital recording apparatus taught in Inoue is a data storage medium having a plurality of tracks), comprising: decoding a first quantity of data that is encoded using an error-correcting code and that spans multiple tracks from the plurality of tracks (the C1 Decoders 44 in Figure 6B of Inoue are used for decoding a first quantity of data, the C1xC2 coded data, that is encoded using the C1xC2 error-correcting code and that spans multiple tracks from the plurality of tracks); writing to ~~the~~ a correction history record to indicate which of the multiple tracks contained errors when the first quantity of data was decoded (col. 6, lines 52-54 in Inoue teach writing error detected information to a register to indicate which of the words in the row directions, i.e., the words in the multiple tracks, contained errors when the first quantity of C1 encoded data was decoded, hence the registers are a correction history record as claimed; Note: rows of the codeword correspond to tracks in a PCM multi-track digital recording); and decoding a second quantity of data that is encoded using the error-correcting code and that spans the multiple tracks, wherein a limited number of data along the ~~of the~~ multiple tracks are decoded as erasures in accordance with the correction history record (C2 Decoder 56 in Figure 6B of Inoue is used for decoding a second quantity of data, the C2 coded data, that is derived from the

originally encoded C1xC2 error-correcting code and that spans the multiple tracks, wherein a limited number of data along the ~~of the~~ multiple tracks are decoded as erasures in accordance with the correction history record; Note: words in the row directions that are labeled as erasures are words belonging to a limited number of tracks that fall within the erasure correcting ability of the code; Note also that C2 encoded data is a subset of the originally encoded C1xC2 error-correcting code, hence is a second quantity of data that is encoded using the C1xC2 error-correcting code).

35 U.S.C. 102(b) rejection of claim 2.

Col. 6, lines 52-54 in Inoue teach writing error detected information to a register to indicate which of the words in the row directions, i.e., the words in the multiple tracks, contained errors when the first quantity of C1 encoded data was decoded, hence the registers are a correction history record as claimed and writing to the record establishes the correction history record.

35 U.S.C. 102(b) rejection of claims 3 and 4.

Col. 10, lines 65-68 in Inoue teach the use of Reed-Solomon codes. Note: a Reed-Solomon code is also a generalized BCH code.

35 U.S.C. 102(b) rejection of claim 5.

See Magnetic Tape 32 in Figure 6C of Inoue.

35 U.S.C. 102(b) rejection of claim 6.

Inoue teaches calculating a weight for each of the multiple tracks, based upon the correction history record (see Erasure Wt Calculation Circuit 50 in Figure 6B of Inoue); and selecting the limited number of the multiple tracks to be treated as erasures based upon the calculated weight for each of the multiple tracks (C2 Decoder 56 in Figure 6B of Inoue is used for decoding a second quantity of data, the C2 coded data, that is derived from the originally encoded C1xC2 error-correcting code and that spans the multiple tracks, wherein a limited number of data along the ~~of the~~ multiple tracks are decoded as erasures in accordance with the correction history record; Note: words in the row directions that are labeled as erasures are words belonging to a limited number of tracks that fall within the erasure correcting ability of the code; Note also that C2 encoded data is a subset of the originally encoded C1xC2 error-correcting code, hence is a second quantity of data that is encoded using the C1xC2 error-correcting code).

35 U.S.C. 102(b) rejection of claim 7.

Col. 6, lines 56-59 in Inoue teaches examining the correction history record to determine a number s of erasure errors that have been found on each of the multiple tracks; and calculating the weight for each of the multiple tracks as a function of the number of ~~times errors~~ s ~~have been found~~ on each of the multiple tracks.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
4. Claims 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue; Toru et al. (US 4336612 A, hereafter referred to as Inoue).

35 U.S.C. 103(a) rejection of claim 8.

Inoue teaches a method of correcting errors in a data storage medium having a plurality of tracks (col. 8, lines 26-68 of Inoue, Note: the PCM multi-track digital recording apparatus taught in Inoue is a data storage medium having a plurality of tracks), comprising: decoding a first quantity of data that is encoded using an error-correcting code and that spans multiple tracks from the plurality of tracks (the C1 Decoders 44 in Figure 6B of Inoue are used for decoding a first quantity of data, the C1xC2 coded data, that is encoded using the C1xC2 error-correcting code and that spans multiple tracks

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from the plurality of tracks); writing to ~~the~~ a correction history record to indicate which of the multiple tracks contained errors when the first quantity of data was decoded (col. 6, lines 52-54 in Inoue teach writing error detected information to a register to indicate which of the words in the row directions, i.e., the words in the multiple tracks, contained errors when the first quantity of C1 encoded data was decoded, hence the registers are a correction history record as claimed; Note: rows of the codeword correspond to tracks in a PCM multi-track digital recording); and decoding a second quantity of data that is encoded using the error-correcting code and that spans the multiple tracks, wherein a limited number of data along the ~~of the~~ multiple tracks are decoded as erasures in accordance with the correction history record (C2 Decoder 56 in Figure 6B of Inoue is used for decoding a second quantity of data, the C2 coded data, that is derived from the originally encoded C1xC2 error-correcting code and that spans the multiple tracks, wherein a limited number of data along the ~~of the~~ multiple tracks are decoded as erasures in accordance with the correction history record; Note: words in the row directions that are labeled as erasures are words belonging to a limited number of tracks that fall within the erasure correcting ability of the code; Note also that C2 encoded data is a subset of the originally encoded C1xC2 error-correcting code, hence is a second quantity of data that is encoded using the C1xC2 error-correcting code). However Inoue does not explicitly teach the specific use of computer stored instructions for implementing the method taught in the Inoue patent.

The Examiner asserts that it would have been an obvious engineering design choice to select a software solution for implementing the method taught in the Inoue patent since

it is well known in the art that software solutions provide an added degree of flexibility over hardware solutions.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Inoue by including use of computer stored instructions for implementing the method taught in the Inoue patent. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of computer stored instructions for implementing the method taught in the Inoue patent would have provided the opportunity to implement the design taught in the Inoue patent based on obvious engineering design choices given a set of system requirements such as flexibility (Note: it is well known in the art that software solutions provide an added degree of flexibility over hardware solutions).

35 U.S.C. 103(a) rejection of claim 9.

Col. 6, lines 52-54 in Inoue teach writing error detected information to a register to indicate which of the words in the row directions, i.e., the words in the multiple tracks, contained errors when the first quantity of C1 encoded data was decoded, hence the registers are a correction history record as claimed and writing to the record establishes the correction history record.

35 U.S.C. 103(a) rejection of claims 10 and 11.

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Col. 10, lines 65-68 in Inoue teach the use of Reed-Solomon codes. Note: a Reed-Solomon code is also a generalized BCH code.

35 U.S.C. 103(a) rejection of claim 12.

See Magnetic Tape 32 in Figure 6C of Inoue.

35 U.S.C. 103(a) rejection of claim 13.

Inoue teaches calculating a weight for each of the multiple tracks, based upon the correction history record (see Erasure Wt Calculation Circuit 50 in Figure 6B of Inoue); and selecting the limited number of the multiple tracks to be treated as erasures based upon the calculated weight for each of the multiple tracks (C2 Decoder 56 in Figure 6B of Inoue is used for decoding a second quantity of data, the C2 coded data, that is derived from the originally encoded C1xC2 error-correcting code and that spans the multiple tracks, wherein a limited number of data along the ~~of the~~ multiple tracks are decoded as erasures in accordance with the correction history record; Note: words in the row directions that are labeled as erasures are words belonging to a limited number of tracks that fall within the erasure correcting ability of the code; Note also that C2 encoded data is a subset of the originally encoded C1xC2 error-correcting code, hence is a second quantity of data that is encoded using the C1xC2 error-correcting code).

35 U.S.C. 103(a) rejection of claim 14.

Col. 6, lines 56-59 in Inoue teaches examining the correction history record to determine a number s of erasure errors that have been found on each of the multiple tracks; and calculating the weight for each of the multiple tracks as a function of the number of times errors s have been found on each of the multiple tracks.

5. Claims 15-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue; Toru et al. (US 4336612 A, hereafter referred to as Inoue) in view of Umemura; Kojiro et al. (US 5708637 A, hereafter referred to as Umemura).

35 U.S.C. 103(a) rejection of claim 15.

Inoue teaches a method of correcting errors in a data storage medium having a plurality of tracks (col. 8, lines 26-68 of Inoue, Note: the PCM multi-track digital recording apparatus taught in Inoue is a data storage medium having a plurality of tracks), comprising: decoding a first quantity of data that is encoded using an error-correcting code and that spans multiple tracks from the plurality of tracks (the C1 Decoders 44 in Figure 6B of Inoue are used for decoding a first quantity of data, the C1xC2 coded data, that is encoded using the C1xC2 error-correcting code and that spans multiple tracks from the plurality of tracks); writing to ~~the~~ a correction history record to indicate which of the multiple tracks contained errors when the first quantity of data was decoded (col. 6, lines 52-54 in Inoue teach writing error detected information to a register to indicate which of the words in the row directions, i.e., the words in the multiple tracks, contained errors when the first quantity of C1 encoded data was decoded, hence the registers are

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a correction history record as claimed; Note: rows of the codeword correspond to tracks in a PCM multi-track digital recording); and decoding a second quantity of data that is encoded using the error-correcting code and that spans the multiple tracks, wherein a limited number of data along the ~~of the~~ multiple tracks are decoded as erasures in accordance with the correction history record (C2 Decoder 56 in Figure 6B of Inoue is used for decoding a second quantity of data, the C2 coded data, that is derived from the originally encoded C1xC2 error-correcting code and that spans the multiple tracks, wherein a limited number of data along the ~~of the~~ multiple tracks are decoded as erasures in accordance with the correction history record; Note: words in the row directions that are labeled as erasures are words belonging to a limited number of tracks that fall within the erasure correcting ability of the code; Note also that C2 encoded data is a subset of the originally encoded C1xC2 error-correcting code, hence is a second quantity of data that is encoded using the C1xC2 error-correcting code). However Inoue does not explicitly teach the specific use of computer stored instructions for implementing the method taught in the Inoue patent.

The Examiner asserts that it would have been an obvious engineering design choice to select a software solution for implementing the method taught in the Inoue patent since it is well known in the art that software solutions provide an added degree of flexibility over hardware solutions. In addition, the Examiner asserts that a tape storage device is a digital device used in data processing systems such as the one in Figure 1 of Umemura. It is obvious to use a digital device in an environment for which it is specifically designed.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Inoue by including use of computer stored instructions for implementing the method taught in the Inoue patent. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of computer stored instructions for implementing the method taught in the Inoue patent would have provided the opportunity to implement the design taught in the Inoue patent based on obvious engineering design choices given a set of system requirements such as flexibility (Note: it is well known in the art that software solutions provide an added degree of flexibility over hardware solutions).

35 U.S.C. 103(a) rejection of claim 16.

Col. 6, lines 52-54 in Inoue teach writing error detected information to a register to indicate which of the words in the row directions, i.e., the words in the multiple tracks, contained errors when the first quantity of C1 encoded data was decoded, hence the registers are a correction history record as claimed and writing to the record establishes the correction history record.

35 U.S.C. 103(a) rejection of claims 17 and 18.

Col. 10, lines 65-68 in Inoue teach the use of Reed-Solomon codes. Note: a Reed-Solomon code is also a generalized BCH code.

35 U.S.C. 103(a) rejection of claim 19.

See Magnetic Tape 32 in Figure 6C of Inoue.

35 U.S.C. 103(a) rejection of claim 20.

Inoue teaches calculating a weight for each of the multiple tracks, based upon the correction history record (see Erasure Wt Calculation Circuit 50 in Figure 6B of Inoue); and selecting the limited number of the multiple tracks to be treated as erasures based upon the calculated weight for each of the multiple tracks (C2 Decoder 56 in Figure 6B of Inoue is used for decoding a second quantity of data, the C2 coded data, that is derived from the originally encoded C1xC2 error-correcting code and that spans the multiple tracks, wherein a limited number of data along the ~~of the~~ multiple tracks are decoded as erasures in accordance with the correction history record; Note: words in the row directions that are labeled as erasures are words belonging to a limited number of tracks that fall within the erasure correcting ability of the code; Note also that C2 encoded data is a subset of the originally encoded C1xC2 error-correcting code, hence is a second quantity of data that is encoded using the C1xC2 error-correcting code).

35 U.S.C. 103(a) rejection of claim 21.

Col. 6, lines 56-59 in Inoue teaches examining the correction history record to determine a number s of erasure errors that have been found on each of the multiple tracks; and calculating the weight for each of the multiple tracks as a function of the number of ~~times errors~~ s ~~have been found~~ on each of the multiple tracks.

35 U.S.C. 103(a) rejection of claim 22.

See Figure 1 in Umemura.

35 U.S.C. 103(a) rejection of claims 23 and 24.

Inoue and Umemura substantially teaches the claimed invention described in claims 15-22 (as rejected above).

However Inoue and Umemura does not explicitly teach the specific use of the data processing system embedded in the storage device.

The Examiner asserts that Inoue and Umemura teach all of the elements of the data storage device and data processing system as claimed in claims 15-22 and an embodiment of the teachings in the Inoue and Umemura patents whereby the processing system is embedded in the storage device is an obvious engineering design choice based on system requirements, for example, VCR for use in audio visual reproduction for a television screen require that the processing system be embedded in the storage device so that digital and audio data is processed before it is outputted to the television screen.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Inoue and Umemura by including use of the data processing system embedded in the storage device. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the data

processing system embedded in the storage device would have provided the opportunity to implement an embodiment of the teachings in the Inoue and Umemura patents for use in audio visual reproduction for a television screen require that the processing system be embedded in the storage device so that digital and audio data is processed before it is outputted to the television screen.

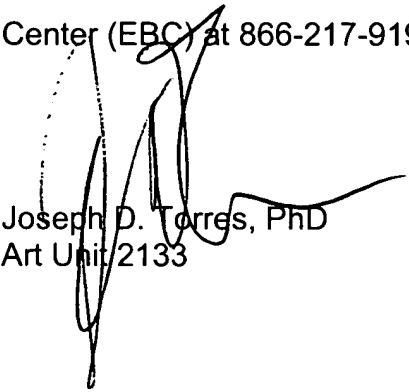
Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gill; Richard A. et al. (US 5255272 A) teaches an error correction apparatus that detects and corrects errors in data read from a magnetic medium such as a magnetic tape.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Art Unit 2133